III–V Nanowire Transistors for Low-Power Logic Applications: A Review and Outlook

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(Review Paper)

***Abstract*— III–V semiconductors, especially InAs, have much higher electron mobilities than Si and have been considered as promising candidates for n-channel materials for post-Si low-power CMOS logic applications. Combined with the inherent 3-D structure that enables the gate-all-around (GAA) geometry for superb gate electrostatic control, III–V nanowire (NW) MOSFETs are well positioned to extend the scaling beyond Si. This paper attempts to provide a review of the growth and fabrication approaches (both bottom–up and top–down), and the state-of-the-art device performance of III-V NW GAA MOSFETs, as well as an outlook of their scaling potential.**

***Index Terms*— III–V, gate-all-around (GAA), MOSFET, nanowire (NW), scaling.**

I. Introduction

III–V SEMICONDUCTOR materials, especially InAs, are known to have a much higher electron mobility than Si [1]–[3]. For extremely scaled FETs, the high mobility is translated to high source-side carrier injection velocity [3]–[5]. III–V transistors, therefore, have been widely used for high-speed and RF electronic applications for decades. Record high-frequency performances have been achieved using III–V channels [6]–[8]. Recently, attention has been drawn on the potential of III–V materials for logic device applications [3], [9]–[11], which has historically been the territory of Si. The continuous performance improvement of Si CMOS ICs over the past 40 years has been enabled by aggressive downscaling of the transistor size, as well as the increase of operating frequency, with the enhancement of power density as a side effect. However, as the device packing density increases drastically, the power dissipation has become a major obstacle that prevents further scaling and performance improvement [12], [13]. Replacing Si with other materials possessing higher carrier mobilities, such as III–Vs, could potentially solve the power issue, because a reduced supply voltage (V_{dd}) may be used to deliver similar or even superior device performance [3]. Del Alamo [3] and Chau *et al.* [10] have given detailed discussions of the challenges and opportunities of III–Vs for CMOS applications.

While switching to a new material system is still at the research stage, the industry has already made a revolutionary change in the geometric structure of CMOS channels. Trigate FinFET devices have been adopted by the industry to replace conventional single-gate planar devices. Among all the different multigate structures, the gate-all-around (GAA) nanowire (NW) structure has the shortest natural length (given the same gate oxide thickness and the same lateral dimensions, i.e., the diameter of an NW, the width of a fin, and the thickness of an ultrathin body) and, therefore, the best gate-length scaling potential [14]. A GAA structure will likely be the solution for ultimately scaled transistors. In this light, we here review several important aspects regarding the development of III–V NW nMOSFETs. Section II discusses and compares different growth/fabrication approaches for III–V NW devices. Section III reviews the diameter-dependent band structures of III–V NWs (mainly on binary InAs) as well as their scaling potential. The OFF-state performance is reviewed in Section IV, while the NW electron mobility and the ON-state performance are reviewed and discussed in Section V. Although the scope of this review is limited to nMOS, it is worth noting that one type of III–V materials, InGaSb, has very impressive hole mobilities and can be potentially used for pMOSFET applications [3].

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II. Growth/Fabrication of III–V NW Devices

A. Bottom–Up, Vertical Vapor–Liquid–Solid Growth

The bottom–up, vapor–liquid–solid (VLS) method, first introduced in [15], is one of the most popular methods for semiconductor NW synthesis. As shown in Fig. 1(a), it utilizes a metal seed particle, usually made of Au, to catalyze and direct the NW growth. Different techniques, including metal–organic chemical vapor deposition (MOCVD), chemical beam epitaxy (CBE), and molecular beam epitaxy, have been used for VLS growth [16]. At certain growth temperature, the seed particle forms with the elements of a semiconductor material (from the vapor phase) a eutectic droplet (liquid phase). As more growth species are introduced, the droplet becomes supersaturated and then the semiconductor material precipitates out in the form of a solid-phase single-crystal NW. In the case of III–V VLS NW growth by MOCVD, trimethylgallium, trimethyl-indium, AsH_3, and PH_3 are most commonly used precursors. The III–V NWs mostly grow along

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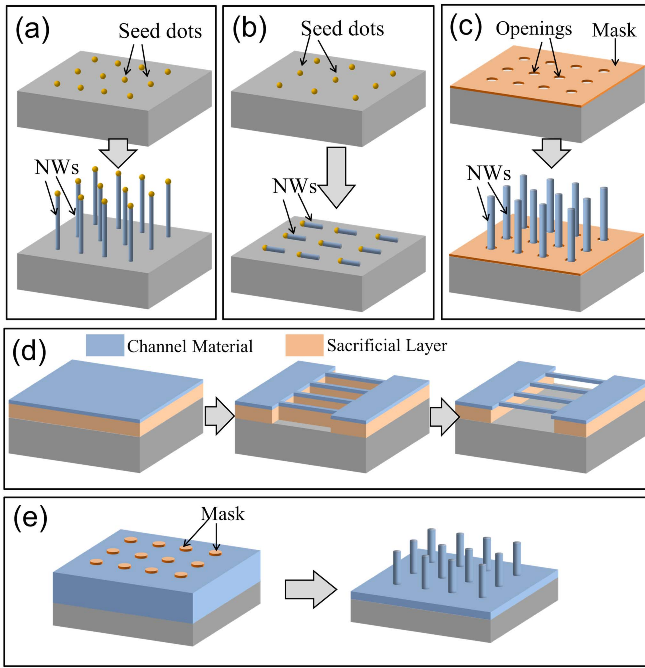

Fig. 1. Schematics of bottom–up and top-down approaches of III–V NW growth/fabrication. (a) Vertical VLS growth. (b) SLE—planar VLS growth. (c) SAE. (d) Top–down planar NWs fabricated by etching the sacrificial layer. (e) Top–down vertical NWs by dry etching.

[111]B direction for energetic reasons [16]. Therefore, vertically aligned NWs can be achieved if a (111) substrate is used [Fig. 1(a)]. VLS growth usually takes place at a temperature much lower than that of the standard thin-film growth such that the thin-film growth, through the vapor–solid (VS) mode, is greatly suppressed. However, the NW growth rate can be high due to the catalytic effect of the seed dots.

The VLS method, as a bottom–up method, holds several distinct advantages. High-aspect ratio NWs with atomically smooth sidewalls and uniform diameters along axial directions can be easily obtained. It is also convenient to scale down the diameter, which is primarily determined by the size of the seed dots. By using colloidal Au dots or metal dots formed through annealing of a thin metal film, VLS InAs NWs with the diameters of less than 20 nm can be readily obtained [17]–[20]. Extremely thin NWs may not grow due to the Gibbs–Thomson effect—loss of supersaturation caused by NW surface energy [21]. However, this does not limit us from obtaining sub-10-nm VLS NW. Jung *et al.* [22] have recently demonstrated sub-10-nm InAs NWs with a minimum diameter of ∼2 nm from Au seeded growth. Ordered NW arrays can be realized by defining Au dots by a lithographical method. Note that due to the formation of hemispherical eutectic droplets, the diameter of the VLS NWs is essentially determined by the volume, instead of the diameter, of the patterned dots (usually having a cylindrical shape) [23]. In this sense, one can reduce the diameter of VLS NWs by only reducing the height of patterned dots, so the lithographical constraint on achieving thin NWs can be relaxed. In addition, heterostuctures along either radial or axial direction can be deterministically incorporated to control the carrier transport property and subthreshold characteristics [24]–[26]. Axial heterojunctions, e.g., InAs/InAsP axial NWs by CBE [24], can be realized by switching ON/OFF growth precursors during VLS growth. Radial junctions usually require a temperature ramp-up in order to enhance the VS growth [27]. The most attractive potential offered by the VLS method is probably the direct integration of III–Vs on a lattice-mismatched substrate, such as silicon. Due to its unique structure, an NW/substrate heterointerface can accommodate more lattice mismatch when compared with planar thin-film interfaces. Below certain critical diameter [28], high-quality NWs can be grown epitaxially on a foreign substrate without generating axial dislocations. This is particularly attractive considering CMOS requires the integration of both n-channel and p-channel materials (such as InAs and GaSb) on one substrate. III–V NWs, including InAs, which is of great interest for the CMOS application for its extremely high electron mobility, have been epitaxially grown on Si (111) [29]. However, the control of growth directions seems to be still challenging for the direct VLS growth on Si. Since Si has a nonpolar crystal structure with all ⟨111⟩ directions being equivalent (in contrast to polar III–V compound semiconductors where there are ⟨111⟩A and ⟨111⟩B [16]), the growth of III–V NWs on Si (111) could happen both the vertical and three slanted ⟨111⟩ directions [29]. We should note that most VLS studies have been done with Au seed dots, which is not compatible with the Si CMOS technology. CMOS-compatible seeds need to be looked into when we consider direct integration of VLS NWs with Si. It is also worth noting that twinning planes as well as a mix of wurtzite (WZ) and zinc blende (ZB) phases alternating along the axial direction are commonly observed in VLS III–V NWs. The phase purity and the planar defect density can be controlled by growth conditions, such as temperature and V/III ratio [30]–[33].

Early proof-of-concept demonstrations of III–V NW transistors are mostly done with VLS NWs [26], [34]. To fabricate a device, vertical NWs were first broken off from the substrate and then randomly dispersed onto an insulating substrate, such as SiO_2/Si, as shown in Fig. 2(a) adapted from [40]. Although impressive performance was achieved, this method cannot be scaled up for chip-level manufacturing.

A breakthrough was demonstrated by researchers from Lund University. They have developed a nontraditional fabrication scheme to make transistors directly on vertical VLS InAs NW arrays, first on InAs native substrates [35], [36], then on Si [37], [38] (with a relatively thick InAs thin-film buffer layer though). Since the transistor channel is vertical, the key fabrication step is to form spacer layers that can separate source and gate as well as gate and drain. A representative device structure is shown in Fig. 2(b), adapted from [35], where SiO_x (formed by angled evaporation) was used as the spacer between the source and the gate. The gate length was defined by the thickness of the gate metal which was also deposited by angled evaporation. Before the drain metallization, a polymer spacer was spin-coated and etched back to expose the tip of the NW. With this kind of fabrication method, array-based NW MOSFETs with an NW diameter of sub-30 nm have been realized [37].

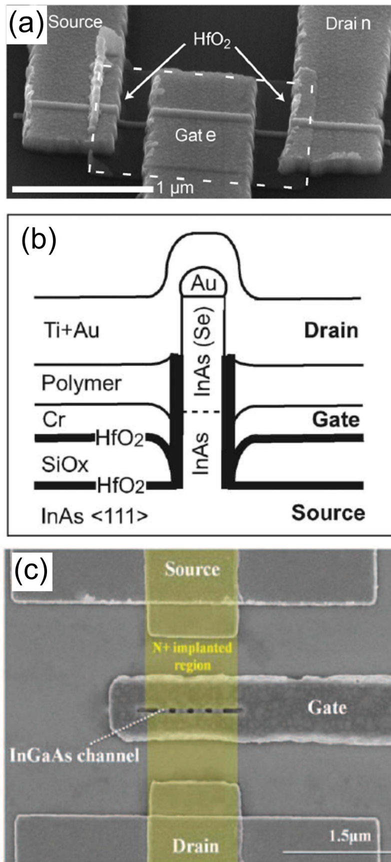

Fig. 2. Different device structures of NW MOSFETs. (a) MOSFET device with an InAs NW channel that is broken off from its original substrate and then dispersed onto a foreign substrate (usually SiO_2/Si). Adapted with permission from [40]. Copyright [2008] IEEE. (b) Vertical VLS NW MOSFETs fabricated by using spacer layers for source/gate and drain/gate separation. Adapted with permission from [35]. Copyright [2008] IEEE. (c) Top–down planar NW MOSFET with p-type NW channels and n^+ implanted S/D. Adapted with permission from [57]. Copyright [2011] IEEE.

Vertically aligned NWs have the potential of achieving a very small transistor footprint. As the top contact is completely isolated from the substrate, the OFF-state leakage current of a vertical NW transistor could be extremely low [39]. The speed performances, however, were shown to be affected by the parasitic capacitances due to large contact pad overlaps [36], [37], [40]. Substantial improvement of RF performance has been shown by using finger contacts to reduce the overlapped area [38]. As the vertical scheme will continue to be developed and assessed by researchers, other challenges include formation of self-aligned source/drain (S/D) (usually achieved in planar devices by S/D implantation or S/D regrowth with gate serving as the mask) and demonstration of its compatibility with even thinner and denser NW arrays. In addition, forming a good ohmic contact directly with the top of the vertical NWs could be challenging as the NWs become even thinner [11] unless a regrown contact region can be developed.

B. Bottom–Up, Selective Lateral Epitaxy

A new, planar type of VLS growth, where the NWs grow in parallel in the plane of the substrate surface, has recently been discovered in [41]. We call this particular VLS growth selective lateral epitaxy (SLE) where the seed particles provide the selectivity. This is schematically shown in Fig. 1(b). For example, GaAs planar NWs are self-aligned bidirectionally along either [0-11] or [01-1] direction if a (100) substrate is used, while unidirectionally aligned planar NWs can be achieved using (110) substrates [42]. We have found that the planar NW growth directions correspond to the projection of out-of-plane ⟨111⟩B directions (standard VLS directions) on the substrate surface [43] and suggested that this is due to the adhesion between liquid-form seed particles and the substrate [44]. Homogeneous SLE of GaAs planar NW arrays with perfect yield have been demonstrated by defining the Au seed dots lithographically [44]. Remarkably, it has been shown that the planar VLS growth can also be applied to heterogeneous epitaxy. High crystalline quality InAs planar NWs with sub-30-nm width have been directly grown on GaAs (100) substrates despite a huge, 7% lattice mismatch [44].

As a VLS method, the planar NW technology shares similar advantages, such as size downscaling, the incorporation of heterostructures, and the potential for heterogeneous integration. Integrating of n-channel and p-channel NWs can be done by multiple patterned VLS growths. The NWs of the first type can be protected by a growth mask (SiO_2 for example) before the seed particles for the second growth are patterned. In particular, unlike the vertical NWs, the planar VLS NWs are compatible with the well-established planar processing technology. Various types of devices, including MESFETs, MOSFETs, and HEMTs, have been demonstrated on homogeneous GaAs planar NWs [27], [45]–[47]. Decent RF performances measured from the array-based GaAs planar NW HEMTs have been reported [48]. For those devices based on homogeneous GaAs planar NWs, the device structure resembles that of a standard planar device except an inherent trigate structure, including the top and two sidewall facets of an NW (the bottom is attached to the substrate).

For the heterogeneous InAs planar NWs grown directly on GaAs, we have developed a method to fabricate GAA NW MOSFETs by releasing the NW channel from the substrate [49]. Due to the competing VS mode during the VLS NW growth, the as-grown InAs planar NW sample [schematically shown in Fig. 1(b)] could be covered by a thin layer of InAs parasitic film across the entire surface. For GaAs planar NWs, the parasitic growth has been minimized to practically zero by optimizing the growth conditions [27], while the current stage of InAs planar growth development left a ∼2-nm-thick parasitic InAs film. In order to perform the undercut etching to release the NW channel, this parasitic InAs film was precisely removed by the digital etching method, which will be explained in more details in Section II-D. The NW channel was then released by selectively etching the exposed GaAs from InAs by a $NH_4OH:H_2O_2:H_2O$ solution. The parasitic film on the S/D region was intentionally kept for improving the contact resistance, which resembled a regrown S/D. The angled sputtering was used to form a conformal gate metal contact. The final device structure is somewhat similar to that of the planar NW MOSFETs fabricated by the top–down etching approach [Fig. 2(c)].

Heterogeneous SLE is a promising technology as it benefits from both bottom–up growth and top–down planar processing technology. Yet it still remains to be shown if it can be done directly on Si, a more desired platform for device integration. Ternary NWs should also be feasible by SLE, where the challenge lies in finding a growth condition that favors the in-plane orientation at the same time allows independent control of the incorporation of two anions or cations. Extensive efforts on growth optimization will be required.

C. Bottom–Up, Selective-Area Epitaxy

The selective-area epitaxy (SAE) approach also produces vertically aligned NW arrays. In contrast to VLS method, it does not rely on any metallic seed dots to guide the growth. Instead, it uses an amorphous mask, usually made of SiO_2, to prevent nucleation on the unwanted area. Small pores are opened on the mask by a lithographical method to expose the surface of the semiconductor substrate underneath, usually of (111) orientation. The vertical NWs grow out of the pores, as shown in Fig. 1(c), and no materials are deposited on the area protected by the mask. In fact, the SAE method has been a long-standing topic for optoelectronic applications [50]. Recently, it has been used to produce vertical NWs for transistor applications [51]–[53]. The SAE growth usually happens in an MOCVD system in order to maintain good growth selectivity and at a growth temperature similar to those of the standard thin-film growth. The diameter of SAE NWs has been shown to be primarily determined by the size of the pore [54], for which the scaling is limited by lithography.

As a bottom–up method, SAE growth shares with the VLS method similar challenges, as well as the advantages, including the heterogeneous integration of lattice-mismatched materials and the flexibility in the incorporation of heterostructures in NWs. In fact, SAE growth of high-In-content InGaAs NWs directly on Si appears to be more successful. The growth of vertically aligned high-yield $In_{0.7}Ga_{0.3}As$ [51] and InAs NW arrays [55] on Si (111) substrates have been realized, demonstrating a significant potential for heterogeneous integration. The high yield was enabled by forming As terminated Si^{3+} surface prior to NW growth. It was found that the huge lattice mismatch (11.6% between InAs and Si) was fully accommodated by the misfit dislocations confined at the heterogeneous interface, resulting in a high-quality, relaxed InAs NW body [55]. In addition, an HEMT-like core–shell structure has been applied to those vertical SAE NWs, leading to a clear improvement of carrier transport characteristics [51]. One important issue of SAE III–V NWs is that the as-grown NWs show strong WZ-ZB polytypism resulting in a large density of stacking faults, which could act as scattering centers. Unlike the VLS method where growth conditions can be tuned to grow phase-pure NWs, stacking-fault-free SAE NWs have not been demonstrated.

The fabrication process of the vertical SAE NW transistors is very similar to that of the VLS NWs. Therefore, the device structure is similar to Fig. 2(b). Yet there are a few reports showing the growth and devices of sub-50-nm NWs by an SAE method, presumably limited by the available lithography technology in an academic institute.

D. Top–Down Approaches

The top–down approach for fabricating III–V NW structures usually starts with a multilayer thin-film structure having a bottom sacrificial layer, which can be selectively etched away in order to release the NWs [56]–[59]. Because of the well-established III–V material system, many selective etchants are known. For example, high Al content AlGaAs can be selectively etched from GaAs by hydrofluoric acid. HCL etches InP but does not attack most other III–V materials, such as InGaAs. Fig. 1(d) shows a generic fabrication process for top–down planar III–V NWs, which was first demonstrated in [57] on an InGaAs/InP structure where the InP substrate served as the sacrificial layer. First, a thin-film heterostructure with the sacrificial layer at the bottom and the channel layer on the top is epitaxially grown. The substrate itself can be the sacrificial layer if a selective etchant can be found. Then, finlike structures can be defined as dry etching, and NWs are formed by etching away the supporting sacrificial layer. Note that since the wet etching is usually anisotropic, the NW orientation can be chosen to facilitate the undercut etching for NW release [57]. An example of the top–down planar NW device structure is shown in Fig. 2(c), adapted from [57]. The InGaAs NWs are p-type doped (during the thin-film growth), whereas the S/D is heavily n-typed doped by ion implantation. Note that although the gate metal contact appears to be wide, the real channel length is defined as the gap between the implanted source and drain areas.

The top–down approach has the advantage of being readily applicable to large-scale manufacturing. Technologies, such as ion implantation and S/D regrowth, can be easily applied. Applying strain for mobility enhancement should also be straightforward. As fabricated from thin films, etched NWs do not contain twining defects or ZB-WZ polytypism, which could be present in bottom–up NWs. In addition, by growing multiple channel/sacrifice layers, vertically stacked NW array could be achieved, creating a new dimension for planar channel integration [59]. As the top–down approach relies on the thin-film growth, this could impose a limit on obtaining very high-In-content InGaAs due to their huge lattice mismatch with the common III–V substrates—GaAs and InP. A thick metamorphic buffer may be used, but it greatly adds the complexity. It is also not so clear how the top–down NWs can be effectively integrated on Si side-by-side with p-channel devices for CMOS applications. In addition, dry-etching-induced surface damage may degrade the transport property.

Recently, top–down chloride-based dry etching was used to produce vertical InGaAs NWs that are similar to those formed by bottom–up growth approaches [60], [61]. NWs as thin as 15 nm have been fabricated by this approach [61]. A schematic is shown in Fig. 1(e), and the device structure resembles that of a bottom–up vertical NW device. The so-called digital etching was used to reduce the surface damage induced by dry etch [60], [61]. The digital etch is a very

precise etching method. Each cycle of digital etch consists of a room-temperature oxidation followed by an oxide removal process. The oxidation, which can be done in an oxygen plasma asher [62] or in a UV ozone tool [63] or by H_2O_2 [64], is a self-limiting process that stops at about 1–1.6 nm beneath the surface depending on the material. Therefore, each etching cycle can precisely remove a very thin layer of material. This is potentially very useful for future fabrication of III–V nanostructures, for example, to precisely thin down the NWs.

III. Band Structure and Scaling Potential

As the gate length of MOSFETs is scaled below 30 nm [65], the diameter of an NW channel, as required by the scaling laws, also has to be in nanoscale. The natural length (λ) that characterizes the scaling behavior of a GAA cylindrical NW structure, given by [66], is

$$\lambda = \sqrt{\frac{2\varepsilon_s d^2 \ln(1 + 2t_{\text{ox}}/d) + \varepsilon_{\text{ox}} d^2}{16\varepsilon_{\text{ox}}}} \tag{1}$$

where ε_s, ε_{ox}, t_{ox}, and d are the dielectric constant of the semiconductor NW, the dielectric constant of the oxide, the thickness of the oxide, and the diameter of the semiconductor NW, respectively. The short-channel effect will be negligibly small if the gate length, L_g, is more than six times larger than λ [14]. If $L_g = 20$ nm, EOT $= 0.6$ nm and assuming an InAs channel with $\varepsilon_s = 15.1\varepsilon_0$, the diameter of the NW needs to be smaller than $\sim$10 nm in order to ensure a good short-channel performance. It is important to understand how the band structures change as the diameter enters the sub-10-nm scale as it is directly related to the threshold voltage shift [67]. Within this size range, III–V NWs are supposed to show clear quantum confinement effect due to their small effective masses. A minimum tolerable d of $In_{0.53}Ga_{0.47}As$ NWs is estimated to be 9 nm in [67] by effective mass approximation considering an acceptable threshold voltage variation of 100 mV induced by the processing variation of NW diameter. In an NW channel, a simple estimation by the effective mass approximation of the bandgap increase ΔE_g due to quantum confinement is [68]

$$\Delta E_g = E_g(d) - E_{g,\text{bulk}} = 2.34\frac{\pi^2\hbar^2}{2d^2 m_e^*} \tag{2}$$

where m_e^* is the electron effective mass ($0.023m_0$ for InAs) and the contribution from the valence band is left out due to the large heavy hole effective mass in III–Vs ($0.41m_0$ for InAs). For InAs NWs, interestingly, both the theoretical calculations [20], [69]–[72] and the experimental results [68] have shown that the effective mass approximation greatly overestimates ΔE_g for $d < 10$ nm. This deviation was attributed to the strong conduction band nonparabolicity in InAs.

Fig. 3 summarizes both theoretical and experimental results on the bandgap of InAs NWs with respect to diameter. As shown in Fig. 3, the effective mass approximation gives a very good estimation of bandgap for $d > 15$ nm, but fails to follow the results calculated by more advanced *ab initio* and $sp^3d^5s^*$ methods. For $d < 10$ nm,

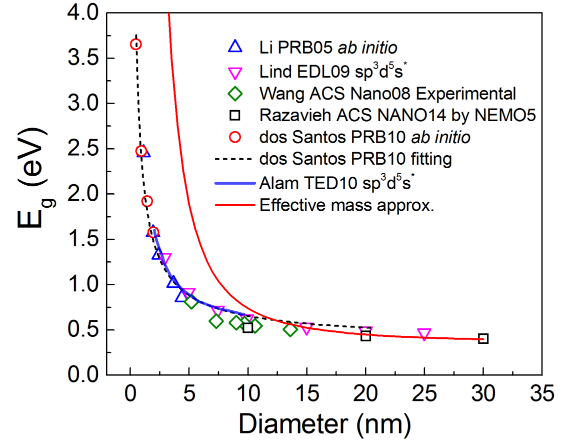

Fig. 3. Summary of theoretical and experimental results on the bandgap of InAs NWs as a function of diameter. The E_g value of bulk InAs is 0.354 eV.

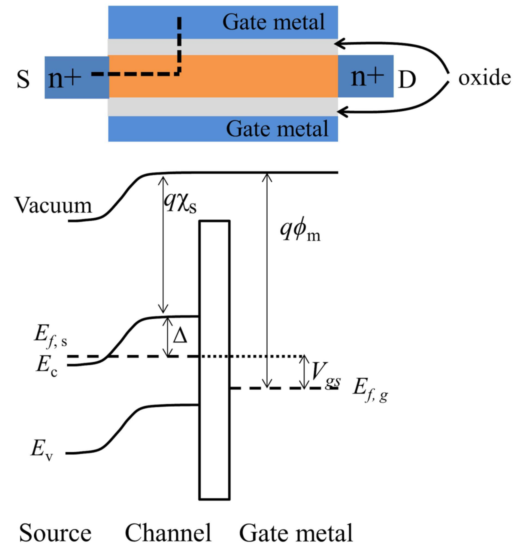

Fig. 4. Schematic of a long-channel NW MOSFET with highly doped source and drain regions. The channel is undoped or lightly doped. Shown at the bottom is the band diagram along the dashed line drawn on the device diagram. The MOSFET is biased in subthreshold.

dos Santos and Piquini *et al.* [72] fitted their *ab initio* data and the experimental results from [68] to yield

$$\Delta E_g = \frac{1.94}{d^{0.81}} \text{ (eV)}. \tag{3}$$

Here, the increase in bandgap follows $d^{-0.81}$ instead of the more aggressive d^{-2}.

Fig. 4 shows the band diagram along the dashed line drawn on the schematic of a long-channel undoped NW MOSFET biased in the subthreshold regime. Following [67] and [73], the bands are essentially flat inside the channel, and no potential drops across the gate oxide, because the mobile charges are negligible in subthreshold (interface-trap charges are not considered). Therefore, the gate voltage V_{gs} can be written as

$$V_{\text{gs}} = \frac{1}{q}(E_{f,s} - E_{f,g}) = \phi_m - \chi_s - \frac{\Delta}{q} \tag{4}$$

where $E_{f,s}$ and $E_{f,g}$ are the Fermi levels of source and gate, respectively. ϕ_m is the gate metal work function, χ_s is the electron affinity of the channel semiconductor, and Δ is the distance between source Fermi level and the conduction band minimum of the channel. Due to the diameter-dependent quantum confinement effect, χ_s can be written as

$$\chi_s = \chi_0 - \frac{\delta E_c(d)}{q} \quad (5)$$

where χ_0 is the bulk electron affinity and $\delta E_c(d)$ is the displacement of the conduction band minimum in an NW, which is approximately ΔE_g for III–Vs. Therefore, (4) becomes

$$V_{\text{gs}} = \phi_m - \chi_0 - \frac{\Delta}{q} + \frac{\delta E_c(d)}{q}. \quad (6)$$

If we define certain Δ to be the threshold condition, the threshold voltage increase due to the diameter downscaling is approximately

$$\Delta V_{\text{gs}}(d) = \frac{\delta E_c(d)}{q}. \quad (7)$$

Note this is a simplified derivation and the result of the more rigorous charge-based analysis can be found in [67]. However, the difference has a very small effect on the analysis below.

Following [67], we calculate for InAs NWs the minimum allowed d limited by the threshold voltage variation due to process variation of d. Similarly as in [67], it is assumed that d has a process variation of $\pm10\%$ and a criteria of $\Delta V_{\text{gs}} < 100$ mV. Using (3), we calculate the minimum tolerable diameter, $d_{\min}$, of InAs NWs is 4.1 nm. If we further assume a 0.6-nm equivalent oxide thickness (EOT) (~3.85-nm HfO_2), the natural length λ is calculated to be 1.55 nm and, therefore, a minimum gate length $L_{g,\min}$ ($=6\lambda$) of ~9 nm for negligible short-channel effect. This shows a good scaling potential for sub-10-nm node technologies [65]. Note that if the effective mass approximation is used for δE_c, $d_{\min}$ and $L_{g,\min}$ are larger, being 12.4 and 23.4 nm, respectively. Although the scaling limit analysis above as proposed in [67] is well accepted, it can possibly be overcome as the processing technology advances.

IV. Subthreshold Performance and Interface-Trap Density

A close-to-ideal subthreshold slope (SS = 60 mV/decade) is desired for modern MOSFETs to achieve low static power dissipation. However, for III–V materials, the interface-trap density D_{it} ($\text{eV}^{-1}\text{cm}^{-2}$) at the oxide–semiconductor interface is usually very high, and it degrades the subthreshold performance. Because of the presence of interface traps, (4) needs to be modified to consider the potential drop across the oxide due to interface charges Q_{it} (C/cm)

$$V_{\text{gs}} = \phi_m - \chi_s - \frac{\Delta}{q} - \frac{Q_{\text{it}}}{C_{\text{ox}}} \quad (8)$$

where C_{ox} (F/cm) is the oxide capacitance per unit length along an NW, which can be written as, for the singe-layer oxide

$$C_{\text{ox}} = \frac{2\pi\varepsilon_{\text{ox}}}{\ln(1+2t_{\text{ox}}/d)}. \quad (9)$$

In the case of multilayer oxides

$$[C_{\text{ox,tot}}]^{-1} = \frac{\ln(1+2t_{\text{ox},1}/d)}{2\pi\varepsilon_{\text{ox},1}} + \frac{\ln(1+2t_{\text{ox},2}/(d+2t_{\text{ox},1}))}{2\pi\varepsilon_{\text{ox},2}} + \cdots \quad (10)$$

Since the drain current I_{ds} is proportional to the mobile charges density, Q_n, near the source which equals $qN_c\exp(-\Delta/kT)$ [74], it is straightforward to conclude from (8) that, for a long channel device ($L_g > 6\lambda$), SS (mV/decade) defined as $dV_{\text{gs}}/d(\log_{10} I_{\text{ds}})$ can be written to be (similarly as in [75] but considering a cylindrical structure)

$$\text{SS} = 60 \cdot \left(1 + \frac{1}{C_{\text{ox}}}\frac{dQ_{\text{it}}}{d(\Delta/q)}\right) \approx 60 \cdot \left(1 + \frac{q\pi dD_{\text{it}}}{C_{\text{ox}}}\right). \quad (11)$$

Therefore, (11) provides a convenient way to estimate D_{it} in a long-channel NW MOSFET. However, we should also note that the other factors that could affect SS are not considered in (11). Other method for D_{it} extraction, such as C–V measurements, cannot be easily implemented on an NW device, especially single-NW transistors.

Fig. 5(a) summarizes SS from the III–V NW MOSFET works [18], [24], [35], [40], [47], [51], [53], [57], [58], [60], [76]–[79]. The SSs are plotted against the ratio between the gate length L_g and the natural length λ, which is calculated by (1). In the case of multilayer oxide, it can be shown by following the original derivation in [66] that:

$$\lambda = \sqrt{\frac{\pi\varepsilon_s d^2}{4C_{\text{ox,tot}}} + \frac{d^2}{16}}. \quad (12)$$

For devices with the MOSHEMT structure, the barrier semiconductor layers are also considered in the calculation of C_{ox}. Relative dielectric constants of 8 [80] and 18 [81] are used for ALD Al_2O_3 and HfO_2, respectively, to obtain EOT. The simulated SS versus L_g/λ taken from [66] (without D_{it}) is also shown in Fig. 5(a) for a comparison with the experimental data. As seen from Fig. 5(a), many experimental data do not follow the simulated results, showing a much higher SS due to high D_{it}. Al_2O_3 has been the most popular dielectric material for III–V MOS devices after high-performance MOSFETs were demonstrated [82], [83]. D_{it} estimated by (11) for the top–down etched vertical $Al_2O_3/In_{0.53}Ga_{0.47}As$ NW devices [60] is 1.9×10^{13} $\text{eV}^{-1}\text{cm}^{-2}$ · $(NH_4)_2S$ solution has been widely used for III–V MOS device interface passivation [84], [85]. With $(NH_4)_2S$ passivation, D_{it} is estimated to be in the middle 10^{12} $\text{eV}^{-1}\text{cm}^{-2}$ range from the top–down planar InGaAs NW devices [58], [59]. Forming gas annealing, a standard approach used to improve the Si/SiO_2 interface, has also been shown effective in improving the Al_2O_3/InGaAs NW interface quality [75]. On InAs bottom–up VLS NWs, both Al_2O_3 and HfO_2 [18], [24], [77], [79] yield a D_{it} great than 2×10^{13} $\text{eV}^{-1}\text{cm}^{-2}$ based on (11). Interestingly, plasma-enhanced chemical vapor deposited (PECVD) SiN_x seems to form a better interface with InAs NWs with an estimated D_{it} of 2.5×10^{12} $\text{eV}^{-1}\text{cm}^{-2}$ [78]. Surprisingly, SAE NW devices do not show much degraded D_{it} (~4×10^{12} $\text{eV}^{-1}\text{cm}^{-2}$ extracted from [51]) compared with the other types of NWs, although SAE NWs do not have a well-defined sidewall facet due to the presence of high-density

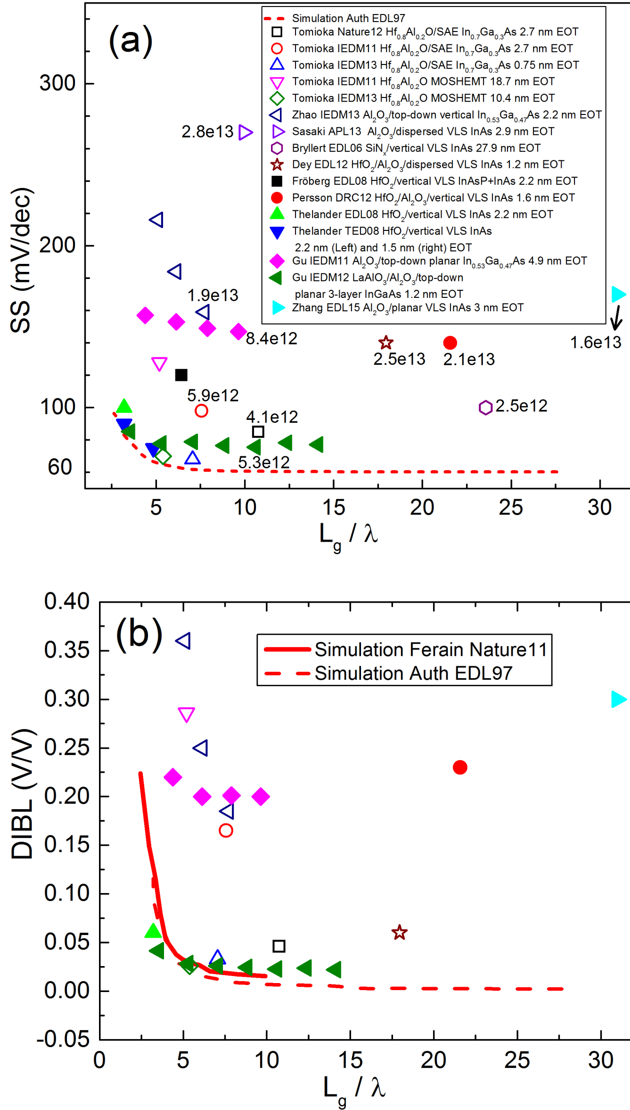

Fig. 5. (a) Plot of SS versus L_g/λ. SS values are taken from experimental results of III–V NW MOSFETs in the literature. Extracted D_{it} numbers in unit of $cm^{-2}eV^{-1}$ have been marked next to long-channel data points. Red dashed line: trend for simulated GAA NW transistors taken from [66]. (b) Plot of experimental DIBLs of III–V NW MOSFETs versus L_g/λ. The symbols in (b) share the same legend as (a). The lines are simulated DIBL data from [14] and [66].

stacking faults. Nonetheless, all those interface-trap densities extracted from NW devices are somewhat larger than the best results from planar devices where a midgap D_{it} in the middle 10^{11} $eV^{-1}cm^{-2}$ range can be achieved [80], [86]. This is presumably related to the difficulty of simultaneously passivating multiple facets that are present in an NW structure. According to [90], the interface properties can be inherently different for different III–V surface orientations given the same oxide material. The GaAs (111)A surface, which is the sidewall facet of the bottom–up planar VLS NWs [46], has been shown to be free of Fermi-level pinning and yield the best MOS interface quality compared with the other surfaces [90]. Given a high D_{it}, EOT needs to be reduced such that C_{ox} is much larger than the capacitance induced by interface traps to get a close-to-ideal SS (11). For example, assuming $D_{it} = 5 \times 10^{12}$ $eV^{-1}cm^{-2}$, an EOT of less than ~0.8 nm can lead to SS of sub-70 mV/decade for long-channel devices. As seen from Fig. 5(a), devices with thin EOTs generally follow the ideal curve more closely.

Two passivation schemes are worth noting here. One is to utilize a radial III–V heterojunction structure. For example, InP, a relatively high-bandgap material in the III–V family, was shown to form a better oxide/semiconductor interface than InGaAs [86]. D_{it} in the low 10^{11} $eV^{-1}cm^{-2}$ range has been demonstrated [86]–[88]. By inserting a thin layer of InP between the gate oxide and the high-mobility InGaAs, the interface quality is expected to be improved. This has been shown in comparative studies on planar devices [89] and also on NWs [26]. Note that an epitaxially smooth interface is desired between InP and InGaAs, so it is preferred that the InP deposition is done monolithically after the NW growth. Bottom–up VLS and SAE technologies are, therefore, better suited for this passivation scheme. Another interesting technology is to use a Si interlayer between the oxide and III–Vs to improve the interface quality. This Si interlayer has been shown to be effective to unpin the GaAs surface Fermi level on both (100) and (111)B surface [91]–[93]. The oxide/Si/InGaAs interface also exhibited a low D_{it} [94]. The Si interlayer is usually deposited by PECVD and has been shown to be effective in removing oxygen from the native Ga_2O_3 [95], which is believed to be responsible for the Fermi-level pinning in the upper half of the GaAs bandgap [90]. This kind of *ex situ* passivation scheme is attractive due to its simplicity and potential for cost-efficient large-scale manufacturing. Although Si interlayer was shown to be effective on GaAs NWs [46], its effectiveness is still to be demonstrated on high-In-content InGaAs NWs.

Fig. 5(b) shows a summary of drain-induced barrier lowering (DIBL) versus L_g/λ in the literature. The symbols share the same legend, as shown in Fig. 5(a). How D_{it} affects DIBL is not so clear as SS and requires some simulation studies. However, we observe from Fig. 5(b) that, in general, a device with low D_{it} [estimated from Fig. 5(a)] and thin EOT follows the ideal curve better.

V. Mobility and On-State Performance

As III–Vs are primarily of interest for their high electron mobility, it is, therefore, very important to examine how the mobility can be preserved in an NW structure, especially how the mobility changes as diameter decreases. The low-field mobility (will hereafter be referred as just mobility) is not only interesting for the fundamental transport study, but it also important for predicting the drain current in short-channel devices. It is directly related to the carrier backscattering coefficient, and the higher it is, the closer a MOSFET device approaches its ballistic limit [96]. Most detailed mobility studies of III–V NWs are based on a VLS method [19], [26], [97]–[101], due to its convenience for preparing NWs with a wide range of diameters and, with several microns in length, which ensures the carrier transport is in the diffusive regime. For the VLS-NW mobility study, back-gated MOSFET devices

with NWs sitting on a SiO_2/Si substrate are commonly used. The so-called field-effect mobility (μ_{FE}) is often extracted from the measured transconductance g_m

$$\mu_{FE} = \frac{g_m L_g}{V_{ds} C_g} \tag{13}$$

where C_g is the total gate capacitance and V_{ds} needs to be small to ensure a low-field condition. Because the thickness of SiO_2 used for the backgate is commonly more than 50 nm in those works mentioned above, the geometric oxide capacitance, C_{ox}, is small compared with the ON-state semiconductor capacitance, C_s. So C_g is oftentimes approximately replaced by C_{ox}. It is worth noting that D_{it} is not considered in those works, so the gate capacitance is somewhat overestimated considering that only free carriers can contribute to the current.

The measurements on the VLS InAs NWs showed a trend where μ_{FE} decreases as the NW diameter, d, reduces [19], [97], [99]. A room-temperature peak μ_{FE} of $\sim$6000 $cm^2/V \cdot s$ was measured for $d = 35$ nm, and it reduced to $\sim$2500 $cm^2/V \cdot s$ for $d = 15$ nm [19]. These numbers are to be compared with $\sim$30 000 $cm^2/V \cdot s$ measured from planar AlSb/InAs quantum wells [102]. The decrease was attributed to the surface roughness scattering as any surface effect would be more pronounced for thinner NWs. Similar trend was also observed in $In_{0.7}Ga_{0.3}As$ NWs [98]. Wang *et al.* [97] also observed a monotonic decrease of peak μ_{FE} when d reduced from $\sim$55 nm to $\sim$22 nm. In addition, they systematically studied the surface roughness effect for a fixed diameter. The sidewall surface rms roughness was measured by atomic force microscopy on NWs that were laid down laterally. It was shown that for NWs with the diameters of $\sim$27 nm, room-temperature peak μ_{FE} decreases from $\sim$8200 $cm^2/V \cdot s$ with rms $\approx$ 0.86 nm to $\sim$1200 $cm^2/V \cdot s$ with rms $\approx$ 1.87 nm. Note that all the above measurements used as-grown NWs covered with a native oxide layer of a couple of nanometers. Gupta *et al.* [100] observed a similar trend for the diameter-dependent mobility in InAs NWs but claimed that surface state scattering, instead of roughness, dominated in their case.

Interestingly, the diameter-dependent mobility has a different trend observed in the well-passivated InGaAs NWs [101], [103]. A high-quality, directly interfaced oxide material or other high-bandgap III–Vs can push the peak of the carrier concentration away from the interface due to a quantum mechanical effect. This could potentially help the mobility improvement. On the other hand, it is questionable if a low-quality native oxide layer could have such an effect. Gu *et al.* [103] observed an increase of the effective electron mobility in their top–down $In_{0.53}Ga_{0.47}As$ NW MOSFETs when the NW width decreases from 50 to 30 nm. They explained the result by the carrier volume inversion. According to their simulation, electrons in a 30-nm-thick NW tends to concentrate more in the center of the NW compared with 50-nm NWs, presumably resulting in a reduced surface effect. Van Tilburg *et al.* [101] also observed an increase of mobility as d reduced in their InAs NWs passivated by a thin InP shell layer, which was monolithically grown after the NW growth. A remarkably high μ_{FE} of 11 500 $cm^2/V \cdot s$ was measured from a similar InAs/InP core/shell structure ($d = 25$ nm)

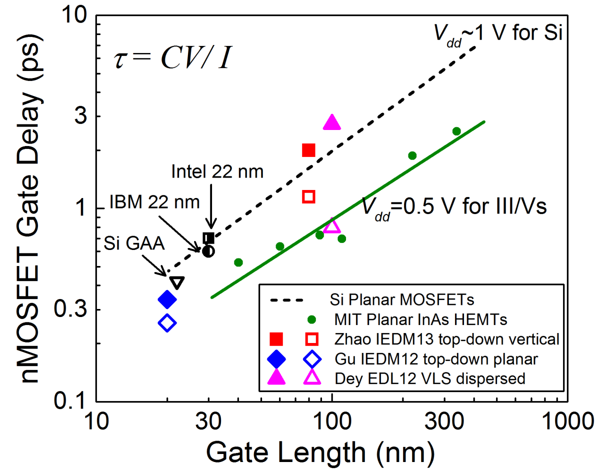

Fig. 6. CV/I gate delays of selected, representative III–V NW MOSFETs [18], [58], [60]. The delays of Si MOSFETs and the state-of-the-art planar III–V devices are also shown (the data are taken from [106]). The open symbols represent the delay calculated by the gate capacitance that rules out the contribution from interface traps, whereas the filled symbols are with D_{it}.

in [26] at room temperature. Those results demonstrate an HEMT-like heterostructure a very attractive method for improving the carrier mobility in III–V NWs. Although the surface-related mobility degradation may eventually take over for extremely scaled NWs, the experimental results above suggest that a well-passivated NW might push the surface-effect-dominated size range toward the smaller end. Overall, the measured mobilities in InAs and InGaAs NWs are substantially higher than those in the inversion layer of a Si MOSFET (typically in the range of several hundred in $cm^2/V \cdot s$ [74]) and those measured from Si NW GAA MOSFETs [104].

Fig. 6 shows the gate delay of the high-performance, representative III–V NW devices calculated by $C_g V_{dd}/I_{dsat}$ (will be referred to CV/I hereafter) [9]. Note that the CV/I delay can be considered intrinsic as it does not consider the parasitic parameters, such as the fringing capacitance. Furthermore, an effective current I_{eff}, which is smaller than I_{dsat}, was shown to give a better estimation of the gate delay [105]. Therefore, CV/I gives a very optimistic estimation. Nonetheless, it is still a useful metric to compare the potential of different technologies as it has been used in [9] and [106]. The CV/I delays of Si MOSFETs of a wide range of technology nodes as well as the delays of the planar InAs HEMT devices are also shown in Fig. 6. Both sets of data are taken from [106]. V_{dd} of the Si data is $\sim$1 V. In addition, the delays of the advanced Intel 22-nm node ($V_{dd} = 0.8$ V) [108] and IBM 22-nm node ($V_{dd} = 1$ V) [109] are calculated and highlighted. The state-of-the-art Si GAA NW MOSFET is also shown [110]. Note that as seen from Fig. 6, the state-of-the-art planar III–V devices have shown a clear advantage in intrinsic delay, remarkably, at a low V_{dd} of 0.5 V.

Following [9], because III–V devices normally do not have an optimized threshold voltage V_{th}, I_{dsat} is taken at $V_{ds} = V_{dd}$ and $V_{gs} = V_{th} + (2/3)V_{dd}$, where V_{dd} is 0.5 V. The gate capacitance, C_g, is obtained from a 2-D Poisson–Schrödinger

TABLE I
I_{ON} COMPARISON BETWEEN III–V AND Si NW DEVICES

	d (nm)	L_g (nm)	Method	I_{on} [a] (μA/μm)	Ref.
Si	12.8	22	Top-down	550 [b]	[110]
InAs	15	100	VLS	400	[18]
InGaAs	~25	20	Top-down	500	[58]

[a] I_{on} is normalized to total perimeter and estimated at $V_{ds} = V_{dd} = 0.5$ V and $V_{gs} = V_{th} + (2/3)V_{dd}$, where V_{th} is extracted from peak g_m method.
[b] I_{on} is about 400 μA/μm if extracted at $V_{dd} = 0.5$ V and I_{off} =100 nA/μm.

coupled simulation of the gate electrostatics at the NW cross section by Nextnano [107]. $D_{\rm it}$, as estimated earlier, is added to capture the gate voltage stretch-out. Note that two data points are shown for each NW device in Fig. 6. The open symbols represent the delay calculated by the gate capacitance that rules out the contribution from interface traps, whereas the filled symbols are with $D_{\rm it}$. As we can see, the open symbols follow better with the trend of the state-of-the-art planar III–V devices (those are HEMT devices that do not have $D_{\rm it}$ effect) and show advantage over the Si MOSFETs. However, $D_{\rm it}$ is seen to substantially corrupt the gate delay as it increases the total gate capacitance and also degrades current, because a substantial portion of channel electrons go to interface states, and therefore does not conduct current.

As the CMOS scaling continues, the parasitic and wiring capacitances have become increasingly significant such that the intrinsic gate capacitance is now not dominating. Therefore, it will also be informative to compare ON-state current at fixed $V_{\rm dd}$. Simulation results have shown that III–V NW devices (especially InAs) do not outperform Si when both operate at their ballistic limit [111]. The reason is that III–Vs have small electron effective mass leading to reduced density of states and, therefore, reduced gate capacitance and inversion charge. Nonetheless, the state-of-the-art planar III–V devices [106], [112] show considerably higher $I_{\rm ON}$ compared with the advanced Si FinFET technology [113] when $I_{\rm ON}$ (at $V_{\rm dd} = 0.5$ V and $I_{\rm OFF} = 100$ nA/μm) is normalized to the actual conducting width. III–V planar devices now operate very close to the ballistic limit [114], while Si devices do not. It is arguable if Si devices can eventually reach the ballistic limit. Those experimental results encourage the continuous research on III–V device, including NWs, for CMOS applications. Table I compares $I_{\rm ON}$ of the best III–V NW MOSFETs to the state-of-the-art Si GAA NW device. Currently, for experimental results, III–V NWs have not shown an advantage over Si in terms of drive current. Further enhancement of current would require a significant improvement of NW/high-k interface quality to both reduce $D_{\rm it}$ and increase mobility.

VI. CONCLUSION

In summary, we have reviewed various aspects of the development of III–V NW transistors. Advantages and challenges of each fabrication approach have been discussed. Although the top–down methods have been prevailing in the industrial manufacture, the bottom–up methods have been developed to a point that is worth some seriously considerations for practical use, given their potential in the heterogeneous integration and convenience for *in situ* passivation through heterostructures. The InAs NWs have been shown to have a very good scaling potential for beyond-10-nm technology node. Despite so, III–V NW MOSFETs with a sub-10-nm diameter still remain to be extensively studied by experiment. High oxide–semiconductor interface-trap density, a long-standing historical problem for III–Vs, still greatly affects both the OFF-state and ON-state performance of III–V NW transistors. Surface passivation by forming an abrupt heterostructure with some other higher bandgap semiconductors, such InP, is highlighted here as a very promising technology for both reducing $D_{\rm it}$ and improving the carrier transport property.

An NW GAA structure is of interest primarily due to its superb gate electrostatics that can allow further gate-length scaling. Yet the speed performance could be affected, because the NW architecture tends to have an increased ratio between the parasitic capacitance and the useful gate capacitance [104]. Note that the parasitic capacitances usually do not scale with the gate length. New innovations in design and processing technologies for maximizing the speed performance of NW transistors are needed in the future development.

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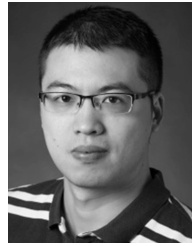

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